Timing Analysis and Optimization of Sequential Circuits

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Recent years have seen rapid strides in the level of sophistication of VLSI circuits. On the performance front, there is a vital need for techniques to design fast, low-power chips with minimum area for increasingly complex systems, while on the economic side there is the vastly increased pressure of time-to-market. These pressures have made the use of CAD tools mandatory in designing complex systems.
Timing Analysis and Optimization of Sequential Circuits describes CAD algorithms for analyzing and optimizing the timing behavior of sequential circuits with special reference to performance parameters such as power and area. A unified approach to performance analysis and optimization of sequential circuits is presented. The state of the art in timing analysis and optimization techniques is described for circuits using edge-triggered or level-sensitive memory elements. Specific emphasis is placed on two methods that are true sequential timing optimizations techniques: retiming and clock skew optimization.
Timing Analysis and Optimization of Sequential Circuits covers the following topics:

- Algorithms for sequential timing analysis
- Fast algorithms for clock skew optimization and their applications
- Efficient techniques for retiming large sequential circuits
- Coupling sequential and combinational optimizations.

Timing Analysis and Optimization of Sequential Circuits is written for graduate students, researchers and professionals in the area of CAD for VLSI and VLSI circuit design.

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